PATENT

Docket No. ___IL-10475___

Assistant Commissioner for Patents

Washington, DC 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of Inventor(s):

Stefan P. Swierkowski

For (title): **A MICROCHANNEL CROSS LOAD ARRAY WITH DENSE PARALLEL INPUT**

1. **Type of Application**

   ■ This new application is for an original patent.

   ☐ This new application is a:

       ☐ Division

       ☐ Continuation

       ☐ Continuation-in-part (CIP)

2. **Benefit of Prior U.S. Application(s) (35 USC 120)**

   ☐ The new application being transmitted claims the benefit of prior U.S. application(s).

3. ☐ **Benefit under 35 U.S.C. 119(e) of United States provisional application(s) listed below:**

   Application Serial No.   Filing Date

4. **Papers enclosed which are required for filing Date Under 37 CFR 1.53(b).**

   _12_ Pages of specification w/cover sheet

   _6_ Pages of claims

   _1_ Pages of abstract

   _3_ Sheets of drawings

       ■ formal

       ☐ informal

5. **Additional papers enclosed**

   ☐ Preliminary Amendment

   ■ Information Disclosure Statement

   ■ Form PTO-1449

6.   **Declaration or oath**

   ■   Enclosed and executed by

   ☐   inventors

   ☐   legal representative of inventor(s) 37 CFR 1.42 or 1.43

   ☐   Not Enclosed

7.   **Assignment**

   ■   An assignment of the invention to <u>The Regents of the University of California</u>.

   ■   is attached

   ☐   will follow

8.   **Certified Copy**

   Certified copy(ies) of application(s)

(country)	(application no.)	(filed)
(country)	(application no.)	(filed)

from which priority is claimed

   ☐   is(are) attached.

   ☐   will follow

9.   **Fee Calculation**

CLAIMS AS FILED					
Type of Claim	Number Filed	Included in Basic Fee	Number Extra	Rate	Total Fee
Total Claims	28	-20 =	8	x $18 =	$ 144.00
Independent Claims	2	-3 =	0	x $78 =	$ 0
			Multiple Claims	=	$ 144.00
			Basic Filing Fee	=	$ 690.00
			Sub-Total	=	$ 834.00
			Small Entity Filing Fee=		**$ 417.00**

10. **Small Entity Statement(s)**

■ Verified Statement that this is a filing by small entity under 37 CFR 1.9 and 1.27 is attached.

Filing Fee Calculation (50% of regular filing fee) $ _____ 417.00

11. **Fee Payment**

☐ Not Enclosed

■ Enclosed (See Account No. Below)

Total Basic Filing Fees To Be Paid $ _____ 417.00
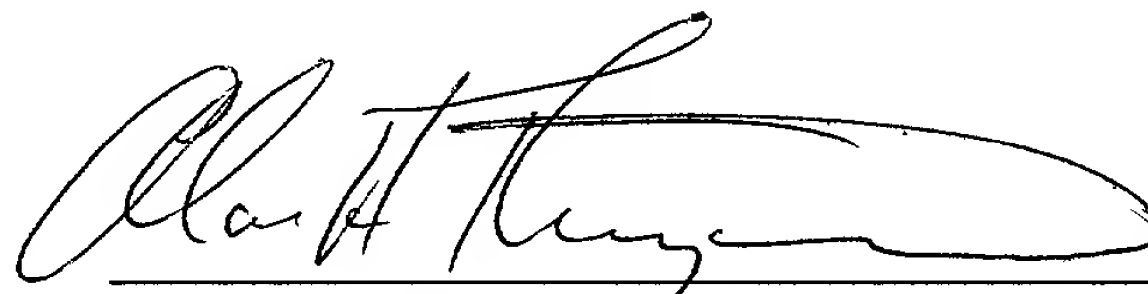
12. **Method of Payment of Fees**

☐ Check in the Amount of $ _____

■ Charge Account No. **12-0695** in the amount of $ **417.00**

A duplicate of this transmittal is attached.

13. **Instructions As To Overpayment/Underpayment**

■ credit/charge

Account No. **12-0695**

☐ refund

Dated: 3/29/00

Alan H. Thompson
Patent Attorney
Registration No. 29,981
P.O. Box 808, L-703
Livermore, CA 94551

Telephone (925) 422-7820

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Stefan P. Swierkowski   Attorney Docket No. : IL-10475
Serial No. :   Art Unit:

Filed :   Examiner:

For : A Microchannel Cross Load Array with Dense Parallel Input

Assistant Commissioner for Patents
Washington, D.C. 20231

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EL269946244US

Date of Deposit___3/29/00___

I hereby certify that the following *attached*

1. Recordation Cover Sheet and Assignment
2. New Application Transmittal (in duplicate)
3. Verified Statement Claiming Small Entity Status
4. Application
   (Specification w/cover sheet 12 pages, Claims 6 pages, Abstract 1 page; Combined Declaration and Power of Attorney; Three (3) sheets of Formal Drawings)
5. Information Disclosure Statement, Form PTO-1449, 3 US Patents
6. Return postcard

is being deposited with the United States Postal Service "Express Mail Post Office to addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box: Patent Application, Washington, D.C. 20231.

Kathy E. Raymond
(Type or print name of person mailing paper)

Kathy E. Raymond

(Signature of person mailing paper or fee)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Stefan P. Swierkowski   Docket No. : IL-10475

Serial No. :   Art Unit :

Filed :   Batch No. :

For : A Microchannel Cross   Examiner :
       Load Array with Dense
       Parallel Input

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS [37 CFR 1.9 (f) and 1.27(d)] - NONPROFIT ORGANIZATION

I hereby declare that I am an official empowered to act on behalf of the nonprofit organization identified below:

> The Regents of the University of California
> 1111 Franklin Street
> Oakland, CA 94607-5200

TYPE OF ORGANIZATION

    X   University or Other Institution of Higher Education

I hereby declare that the nonprofit organization identified above qualifies as a nonprofit organization as defined in 37 CFR 1.9(e) for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code with regard to the invention entitled <u>A Microchannel Cross Load Array with Dense Parallel Input</u>

by inventor(s) <u>Stefan P. Swierkowski</u>

described in

    X   the specification filed herewith.

___   application serial no. _____, filed _____.

___   patent no. _____, issued _____.

I hereby declare that rights under contract or law have been conveyed to and remain with the nonprofit organization with regard to the above identified invention, except for a license to a Federal Agency pursuant to 35 USC 202(c) (4).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

   __X__   no such person, concern, or organization
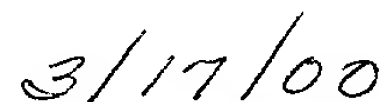
I acknowledge the duty to file, in this application or patent, notification of any charge in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

JANET G. TULK
Laboratory Counsel
Lawrence Livermore National Laboratory
7000 East Avenue, L-701
Livermore, CA 94550

Janet G. Tulk   3/17/00
JANET G. TULK   Date

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A MICROCHANNEL CROSS LOAD ARRAY WITH DENSE PARALLEL INPUT

BY

Stefan P. Swierkowski   (USA)
1655 Warsaw Avenue
Livermore, CA 94550

A MICROCHANNEL CROSS LOAD ARRAY WITH DENSE PARALLEL INPUT

BACKGROUND OF THE INVENTION

5   The present invention relates to loading of microchannel arrays, particularly to T or Cross (+) loading for microfluidic applications, and more particularly to an architecture for T or cross loading that enables a very dense layout of arrays of functionally identical shaped channels.

There are two main types of injection methods in microchannel

10   electrophoresis. The first type is analogous to that used in discrete capillaries where the sample is introduced directly into the end of the microchannel, and there is one physical sample input port per channel. This has been used extensively, and is referred to as electrokinetic (ek) single port injection. The amount of sample actually injected into the column is a strong function of sample

preparation, loading volume, input port shape and volume, exact loading placement, loading field and time, excess sample removal, holding time, etc. which may be hard to control.

5   The second type is a volumetric type of load called T load or Cross load, where the sample plug at the intersection of two microchannels is injected into the column. This type is exemplified by U.S. Patent No. 5,900,130 issued May 4, 1999 to D. Benvegnu, et al. This load type is fundamentally controlled better by the geometry of the intersection, but now the number of input ports per channel has increased from one to three: sample, waste, and cathode. Ek effects
10   may be present or used in the cross load, but the fundamental determinant of the amount of sample loaded and injected is the geometrical volume of the channel intersection, which is subsequently swept out by the running or separation field. The increased space required for additional input ports and the need to electrical bias all of them independently and initially fill them all with sieving media is
15   geometrically and procedurally fraught with practical difficulties – especially for very high density arrays.

The present invention addresses these geometrical and practical operational difficulties. The invention provides an architecture or layout composition which enables a very dense layout of arrays of functionally identical
20   shaped channels. The invention also simultaneously enables efficient parallel shapes and biasing of input wells, waste wells, and bias wells at the input end of the separation columns.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a microchannel cross load array with dense parallel input.

A further object of the invention is to provide a unique architecture for microchannel arrays using T or Cross loading for electrophoresis.

Another object of the invention is to provide a T or Cross loading architecture which enables a very dense layout of arrays of functionally identical shaped channels.

Another object of the invention is to provide an architecture for microfluidic configurations that simultaneously enables efficient parallel shapes and parallel biasing of the input wells, waste wells, and bias wells at the input end of microchannel separation columns.

Other objects and advantages of the present invention will become apparent from the following description and accompanying drawings. The present invention involves an architecture or layout composition for microchannel T or Cross (+) loading to enable dense parallel input for electrophoresis or other injection and separation chemistry experiments that are preformed in microfluidic configurations. The present invention is an architecture for microchannel arrays using T or Cross loading which solves prior problems associated with very high density arrays. The invention provides a way to layout a dense array of similar cross loaders so that high channel densities result, and a minimum member of access holes is used by sharing holes

in the multiple channel layout. This invention uses unique geometrical pattern shaped channels and packing of the layout, taking advantage of several mirror symmetries in the layout, and enables the use of the Cross loader, such as described in about-referenced Patent No. 5,900,130, in dense practical arrays.

5   Based on this layout, experiments show that for the large microchannel array fabrication technology that is currently known, over 1000 channels can be formed on one plate. The architecture of this invention utilizes the Cross loader of the above-referenced patent which consists of two intersecting microchannels (four arms), and provides a package or layout of building blocks in a practical way for

10   a very high density planar integrated array.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated into and form a part of the disclosure, illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention.

Figures 1A and 1B illustrate the basic prior art Cross loaders.

15   Figures 2A, 2B, and 2C illustrate T and Cross loaders made in accordance with the present invention with Figure 2A being generally similar to Figures 1A and 1B.

Figure 3 illustrates an embodiment of a T load architecture of the present invention using circular holes with common rows.

20   Figure 4 illustrates an embodiment of a T load architecture of the present invention that enables the access hole array to be formed on a biaxial,

collinear grid suitable for EDM machining (square holes), with common rows and columns.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides an architecture for microchannel arrays using T or Cross loading which enables dense parallel inputs for

5   electrophoresis or other microfluidic applications. The invention provides a way to layout a dense array of similar Cross loaders so that high channel densities result, and a minimum member of access holes is used by sharing holes in the multiple channel layout. The invention uses unique geometrical packing of the layout, taking advantage of several mirror symmetries in the layout. This

10   architecture is a way to enable the use of the prior art Cross loader into dense practical arrays. An initial layout made in accordance with the present invention shows that for the large microchannel array fabrication technology that now exists, one could make over 1,000 channels on one plate. In addition, the present invention solves the problem of simultaneously enabling efficient parallel shapes

15   and biasing of the input wells, waste wells, and bias wells at the input end of the separation columns.

Referring now to the drawings, Figure 1A and 1B illustrate the basic Cross load, such as described in above-referenced patent No. 5,900,130. When arrays of this type of layout are made, the configuration of the sample (S), waste

20   (W), and cathode (C) input holes is very inconvenient or impractical for the external fluidic reservoirs and biasing electrodes, especially for very dense and

large arrays; the dense intermixed ports require many separate fluidic seals and electrodes. Also, bending or differences in shape of the separation channel is very undesirable (resolution loss).

5   The key to this invention is the distortion of the fluidic path shapes and the changes in length, especially on the waste and cathode paths, and the use of multiple mirror image segments and the arrangement of the input ports so that the ports are arranged in common groups. With the common groups of input ports arranged in parallel rows, it becomes possible to access them with a few o-ring sealed reservoirs; this enables common excess fluid purging without

10   cross contamination, and enables common electrical electrodes to be employed. This makes practical fill fixtures and loading apparatus possible; such can even be formatted to be consistent with the common titer array pitch density. This layout also enables the use of a common slot for the cathode (C) and anode (A) groups.

15   Figure 2A, 2B, and 2C illustrate the evolution of the geometric or architectural design of this invention in the transition from conventional layout (Figure 2A) to the preferred layout of Figure 2C. A key concept is to take separate portions of Figure 2C and use both vertical and horizontal mirror images of those segments and to re-assemble them into arrays with rows and

20   spacings that are compatible with input port fabrication and practical shaped fill reservoirs, such as shown in the embodiments of figures 3 and 4.

Some of the key concepts of the present invention are:

1. Each electrode type is arranged in rows, so that the fluid reservoirs are easy to build.

2. The row arrangement allows a common bias electrode to be used, simplifying input loading fixtures.

5   3. The different flow channels and input structures have functionally identical shapes; thus being very important for uniform separation, filling, loading, injection, purging, refill, etc.

4. The architecture of the embodiment of Figure 3 allows perfectly identical functional shapes. The holes may be square, round, or tapered.

10   5. The embodiment of Figure 4 allows the waste holes to be colinear with the sample holes, i.e., in the same column, and thus in turn, enables fabrication by EDM machining or similar x-cut, y-cut machining for the mandrel; this allows very precise, small practical hole fabrication in very dense and large arrays. The holes may be square, round, or tapered.

15   6. Folded, nested waste path; equal in length to the cathode, if desired.

7. Short sample to cross path allowed (more thorough purging where it matters most, and quick load – ek or hydraulic pressure load).

8. Offset cross intersection allowed.

9. A minimum number of 1.5 holes per channel is needed.

20   10. The separation channels can be made straight (double output pitch) or virtually straight (single output pitch).

11. Sheath flow readout is enabled with a single or double plate cut at the anode (A) end.

Figure 3 illustrates an embodiment of a Cross or T load architecture, similar to that shown in Figure 2C, which uses circular holes or wells with

5 common rows, but not columns; this allows the flow paths for each channel 1-8 to be identical in shape, using multiple mirror image pieces. The flow path from the Cross or T, indicated at 10, to the cathode 11 and to waste 12 are equal in length; the sample 13 to the cross 10 length is short compared to the other flow paths, but could be made much longer, or could have a junction offset for a

10 bigger injection plug. Note that there is only one (1) waste hole 12 for each pair of channels. By way of example, the channel pitch, indicated by arrow Pch, is about 0.5-4.5 mm; and the sample pitch, indicated by arrow Ps is about 2Pch. The hole row spacing from cathode 11 to waste 12, indicated by arrow CW; from waste 12 to sample 13, indicated by arrow SW, and from sample 13 (first row) to

15 sample 13 (second row), indicated by arrow SS, can be adjusted to accommodate load fixtures. The hole row spacing from sample 13 to anode 14, indicated by arrow SA, may be 2-500 mm. Each row has a common bias during operation. The cathode row 11 and distant anode row 14 are each common slots. The flow paths of each of channels 1 through 8 which extends from a sample hole 13 to the

20 anode 14 holes as the number of sample holes. The cathode row 21 and distant anode row 24 are common slots. The holes 25 and 26 on the ends of the waste row 12 and the sample rows 23, are formed in the EDM process (orthogonal rows

and columns) but are not used. Other machining processes producing

orthogonal rows and columns may be used (e.g., conventional NCM - 1 feature at

a time).

By way of example, sample holes 23 and excess holes 26 may have

5   sides of a width in the range of 0.3 mm to 3 mm, waste holes 22 and excess hole

25 may have sides of a width in the range of 0.3 mm to 3 mm, cathode 21 may be

a depth of 0.5 mm to 5 mm and width of 0.5 mm to 2 mm; and anode 24 may

have a depth of 0.5 mm to 5 mm and width of 0.5 mm to 2 mm. Take flow paths

1-8, from injection points 20 to anode 24 may be a length of 2 mm to 500 mm;

10   from injection points 20 to wastes 22 may have a length of 2 mm to 20 mm; from

injection points 20 to cathode 21 may have a length of 2 mm to 20 mm; and from

samples 23 to injection points 20 may have a length of 0.3 mm to 3 mm. The

sample wells may be circular and waste wells may be square, but not by simple

EDM process. A glass ultrasonic drill mandrel tool could be made with square

15   bits and round bits on the same plate with far more effort and with less accuracy.

It has thus been shown that the present invention provides a geometry,

architecture, topology, or layout composition for microchannel arrays using T or

Cross loading for electrophoresis or other injection and separation chemistry

experiments that are performed in microfluidic configurations. This architecture

20   or geometry enables a very dense layout of arrays of functionally identical

shaped channels. It also solves the problem of simultaneously enabling efficient

parallel shapes and biasing of the input wells, waste wells and biasing wells at

the input end of the separation columns. This invention establishes that for large

microchannel array may have an overall length of 2 mm to 500 mm, for example,

with the channels 1-8 having a width of 0.02 mm to 0.30 mm and depth of 0.02

mm to 0.15 mm. The sample holes 13, and waste holes 12 may have a diameter

5   of 0.3 mm to 2 mm, with the common slots of cathodes 11 and anodes 14 having

a width of 0.5 mm to 2 mm. While only sixteen (16) channels and associated

sample hole, with only eight (8) waste holes have been illustrated for simplicity,

numerous additional channels, etc. may be formed on the same plate, as pointed

out above. The flow paths from the injection point to the cathode and from the

10   injection point to the waste wells may be equal or unequal.

Figure 4 illustrates an embodiment of a Cross or T load architecture of

the present invention generally similar to Figure 3, but which enables the access

hole or well array to be formed on a biaxial, collinear grid suitable for Electric

Discharge Machining (EDM) machining (square holes), with common rows and

15   columns. In the scheme, the major difference is the input sample and waste holes

are in common columns, rather than in staggered columns as in Figure 3. The

asymmetric flow paths from injection Cross or T 20 to cathode 21 and waste 22

can still be made the same lengths, just different shapes. The channel pitch,

indicated by arrow Pch is about 0.5-4.5 mm; and the sample pitch, indicated by

20   arrow Ps equals 2Pch, as in Figure 3. The hole spacings from waste 22 to cathode

21, indicated by arrow CW; from waste 22 to a top row of sample 23, indicated

by arrow SW; and from the top row of sample 23 to a lower row of sample 23,

indicated by arrow SS, can be adjusted to accommodated load fixtures. The

spacing from lower row of sample 23 to anode 24, indicated by arrow SA, is 2

mm to 500 mm, for example. Each row has a common bias during operation.

Note that there are only half the number of waste fabrication technology, at least

5 1000 channels can be formed on one plate, thus providing a layout for a dense

array of similar Cross or T loaders so that high channel densities result, and a

minimum number of access holes are used by sharing holes in the multiple

channel layout. The architecture of the present invention can be utilized for

example, in capillary electrophoresis, chemical flow injection analysis, liquid

10 chromatography, enhanced electrokinetic injection, chemical reaction micro

capillary flow systems, combinatorial wet chemistry processing and analysis,

microsample array preparation, etc. The architectural arrangement of this

invention thus extends the use of T or Cross loads with the prior known

problems associated with the use of such loads for dense parallel inputs. The

15 sample and waste wells may have tapered walls for ease of sample

needle/pipette array insertion.

While particular embodiments of the present invention have been

illustrated and/or described, along with various parameters, etc., to exemplify

and teach the principles of the invention, such are not intended to be limiting.

20 Modifications and changes may become apparent to those skilled in the art, it is

intended that the scope of the invention be limited only by the scope of the

appended claims.

THE INVENTION CLAIMED IS

1. A microchannel Cross load array, comprising:

a cathode

an array of sample wells,

an array of waste wells, said sample well comprising twice the number

5   of waste wells,

an anode, and

an array of functionally identical channels, each channel having an

injection point with one well of said array of sample wells, one well of said array

of waste wells, said cathode and said anode.

2. The microchannel Cross load array of Claim 1, which said cathode

and said anode each define common slots.

3. The microchannel Cross load array of Claim 1, wherein said sample wells with parallel sides are selected from the group to define substantially circular holes, tapered holes, and holes.

4. The microchannel Cross load array of Claim 1, wherein said waste wells define substantially circular holes.

5. The microchannel Cross load array of Claim 1, wherein both said sample and waste wells define substantially circular holes.

6. The microchannel Cross load array of Claim 1, wherein said sample wells define substantially square holes.

7. The microchannel Cross load array of Claim 1, wherein said waste wells define substantially square holes.

8. The microchannel Cross load array of Claim 1, wherein both said sample and waste wells define substantially square holes.

9. The microchannel Cross load array of Claim 1, wherein both said sample and waste wells are formed on a biaxial, collinear grid by EDM machining or other machining process producing orthogonal rows and columns.

10. The microchannel Cross load array of Claim 1, wherein said channels are identical in shape.

11. The microchannel Cross load array of Claim 1, wherein said array of channels form flow paths for each channel which are identical in shape, using multiple mirror image pieces.

12. The microchannel cross load array of Claim 1, wherein said array of channels form equal or unequal flow paths from said injection point to said cathode and from said injection point to said waste wells.

13. The microchannel Cross load array of Claim 1, wherein said array of channels from symmetric flow paths from said injection point to said cathode and to said waste wells.

14. The microchannel Cross load array of Claim 13, wherein said symmetric flow paths are of the same lengths.

15. The microchannel Cross load array of Claim 1, wherein said array of sample wells are located in a plurality of rows.

16. The microchannel Cross load array of Claim 15, wherein adjacent channels which are located adjacent said anode have a pitch, Pch, wherein adjacent sample wells in each row have as pitch, Ps, and wherein Ps equals 2Pch.

17. The microchannel Cross load array of Claim 16, wherein the pitch, Pch, is about 0.5-4.5 mm.

18. The microchannel Cross load array of Claim 15, wherein each row of sample wells has a common bias.

19. The microchannel Cross load array of Claim 1, wherein said array of waste wells are located in a row, and have a common bias.

20. An architecture for microchannel arrays using T or Cross loading for injection and separation chemistry applications performed in microfluidic configurations,

said architecture producing a dense layout of functionally identical shaped microchannels, sample wells, and waste wells, and including a common cathode and a common anode,

said microchannels each having an injection point interconnecting a sample well, a waste well, a cathode and an anode,

said microchannels each defining equal length flow paths between said
injection point and said waste, and between said injection point and said
cathode.

21. The architecture for microchannel arrays of Claim 20, wherein said
flow paths are symmetric.

22. The architecture for microchannel arrays of Claim 20, wherein said
sample wells are located in a plurality of rows, and wherein said waste wells are
located in a single row.

23. The architecture for microchannel arrays of Claim 20, wherein said
microchannels each include flow paths from said injection point to a sample well
and from said injection point to said anode.

24. The architecture for microchannel arrays of Claim 23, wherein
adjacent flow paths of said channels located adjacent said anode have a channel
pitch, Pch, wherein adjacent sample wells have a sample pitch, Ps, and wherein
Ps = 2Pch.

25. The architecture for microchannel arrays of Claim 24, wherein the
channel pitch, Pch, is about 0.5-4.5 mm.

26. The architecture for microchannel arrays of Claim 20, wherein said sample wells and said waste wells having a configuration selected from the group consisting of circular and square shapes with straight or tapered walls.

27. The architecture for microchannel arrays of Claim 20, wherein said common cathode and said common anode are each of a slot configuration.

28. The architecture for microchannel arrays of Claim 20, wherein said sample well are located in a plurality of rows, wherein said waste wells are located in a single row, and wherein each of said rows has a common bias.

ABSTRACT OF THE DISCLOSURE

An architecture or layout for microchannel arrays using T or Cross (+) loading for electrophoresis or other injection and separation chemistry that are performed in microfluidic configurations. This architecture enables a very dense layout of arrays of functionally identical shaped channels and it also solves the

5   problem of simultaneously enabling efficient parallel shapes and biasing of the input wells, waste wells, and bias wells at the input end of the separation columns. One T load architecture uses circular holes with common rows, but not columns, which allows the flow paths for each channel to be identical in shape, using multiple mirror image pieces. Another T load architecture enables the

10   access hole array to be formed on a biaxial, collinear grid suitable for EDM micromachining (square holes), with common rows and columns.
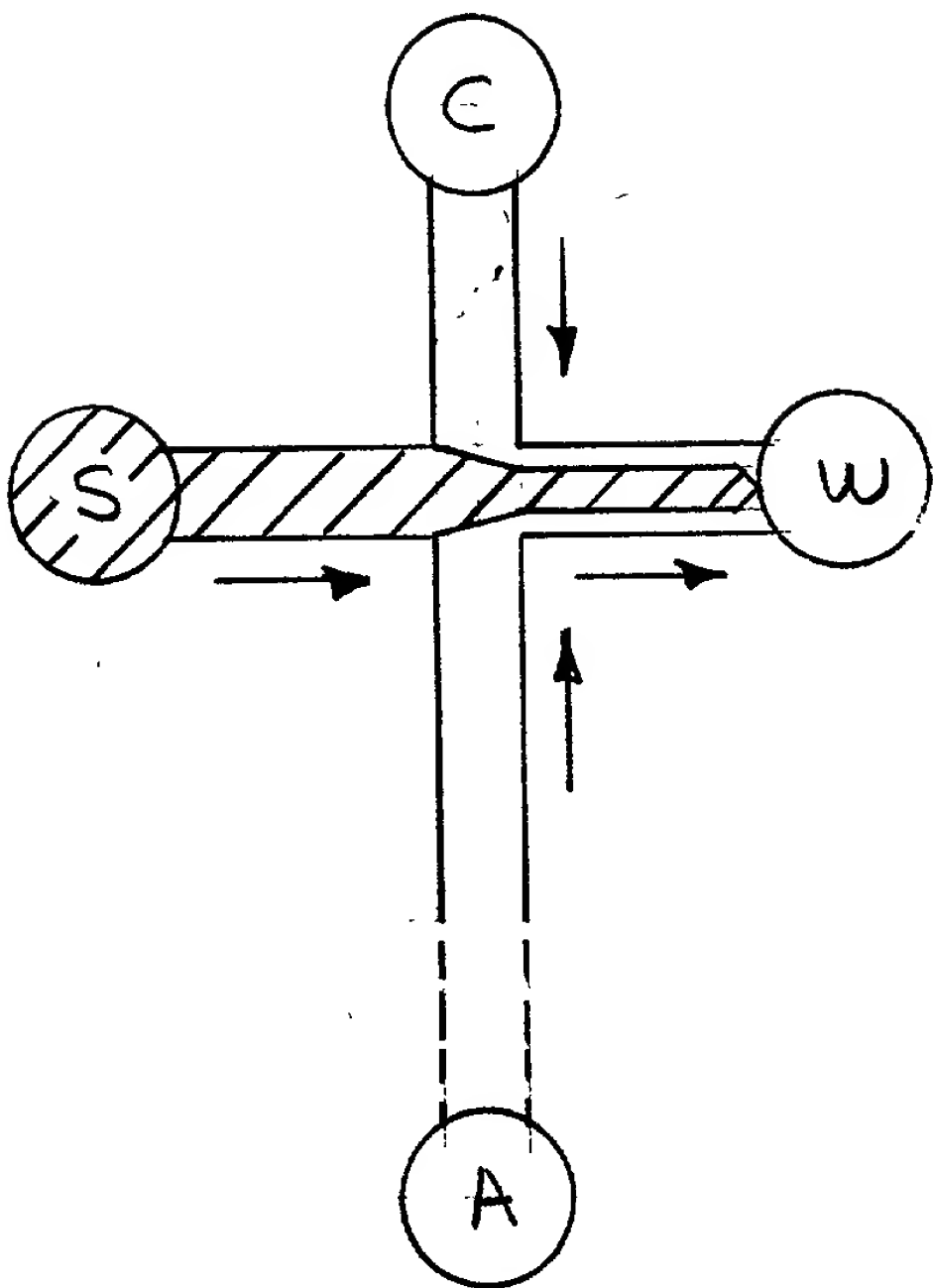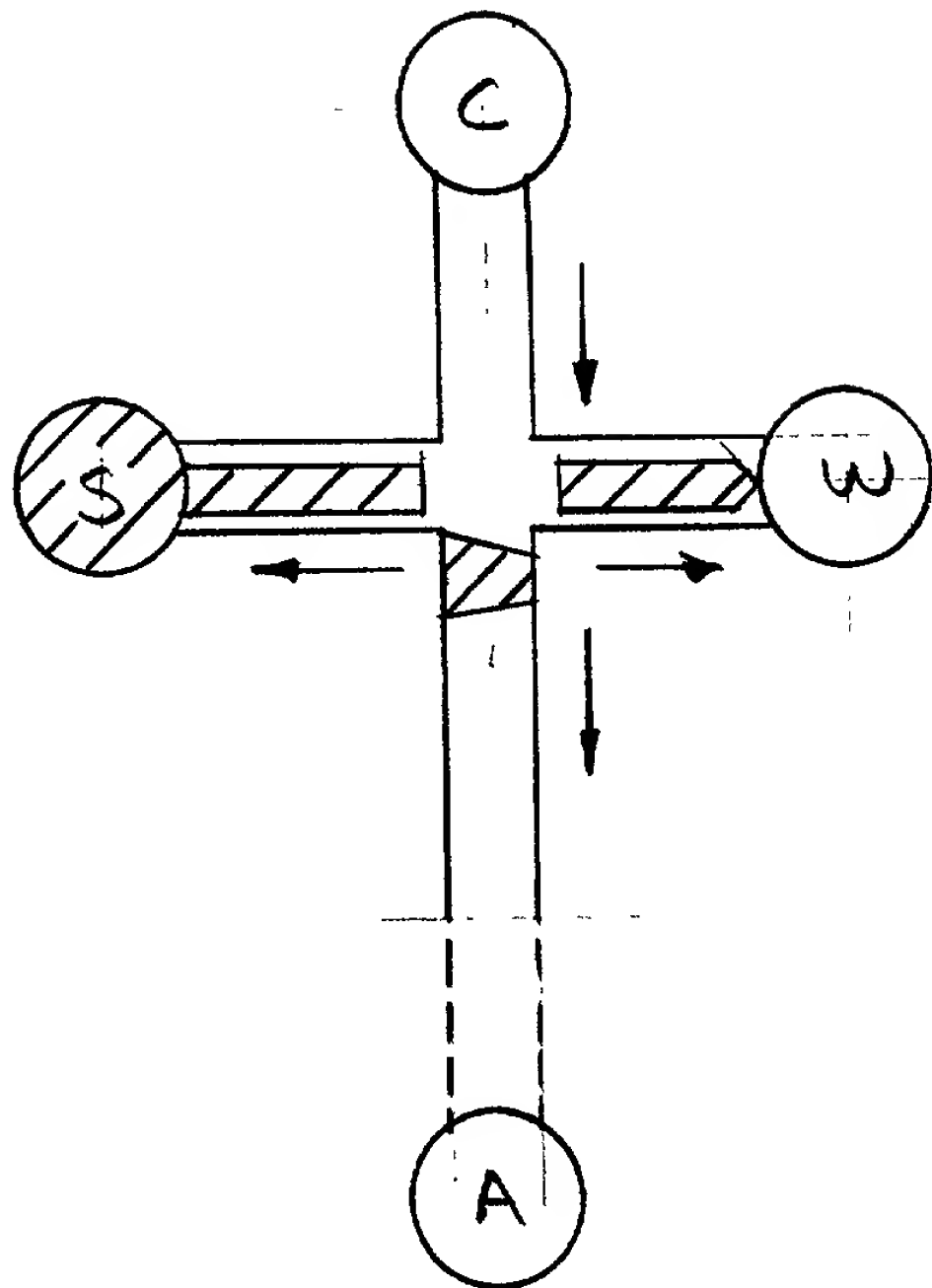
FIG.1
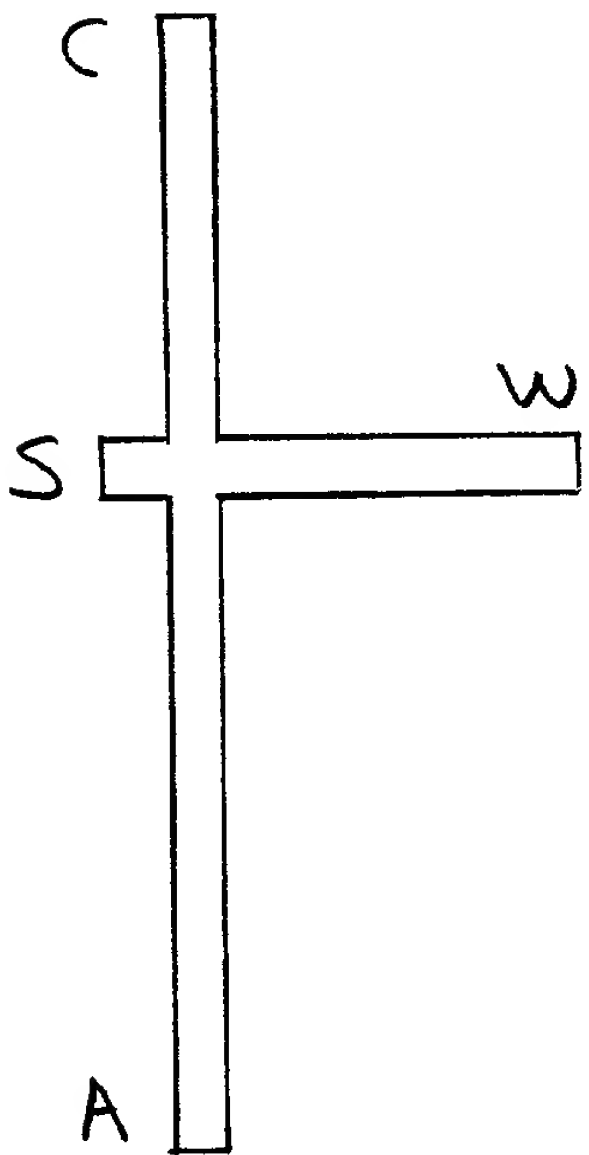
(PRIOR ART)

FIG.1

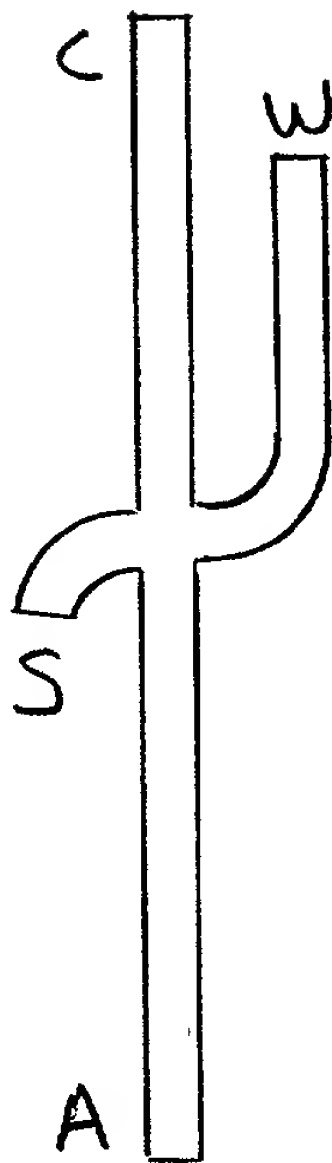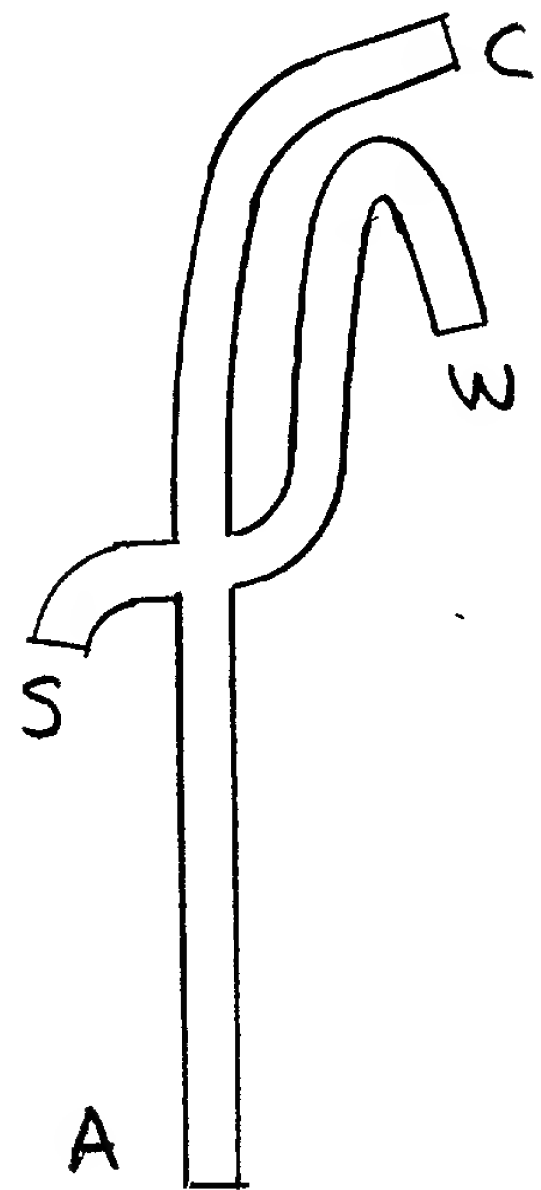(PRIOR ART)

FIG. 2

FIG. 2

FIG. 2

FIG. 3
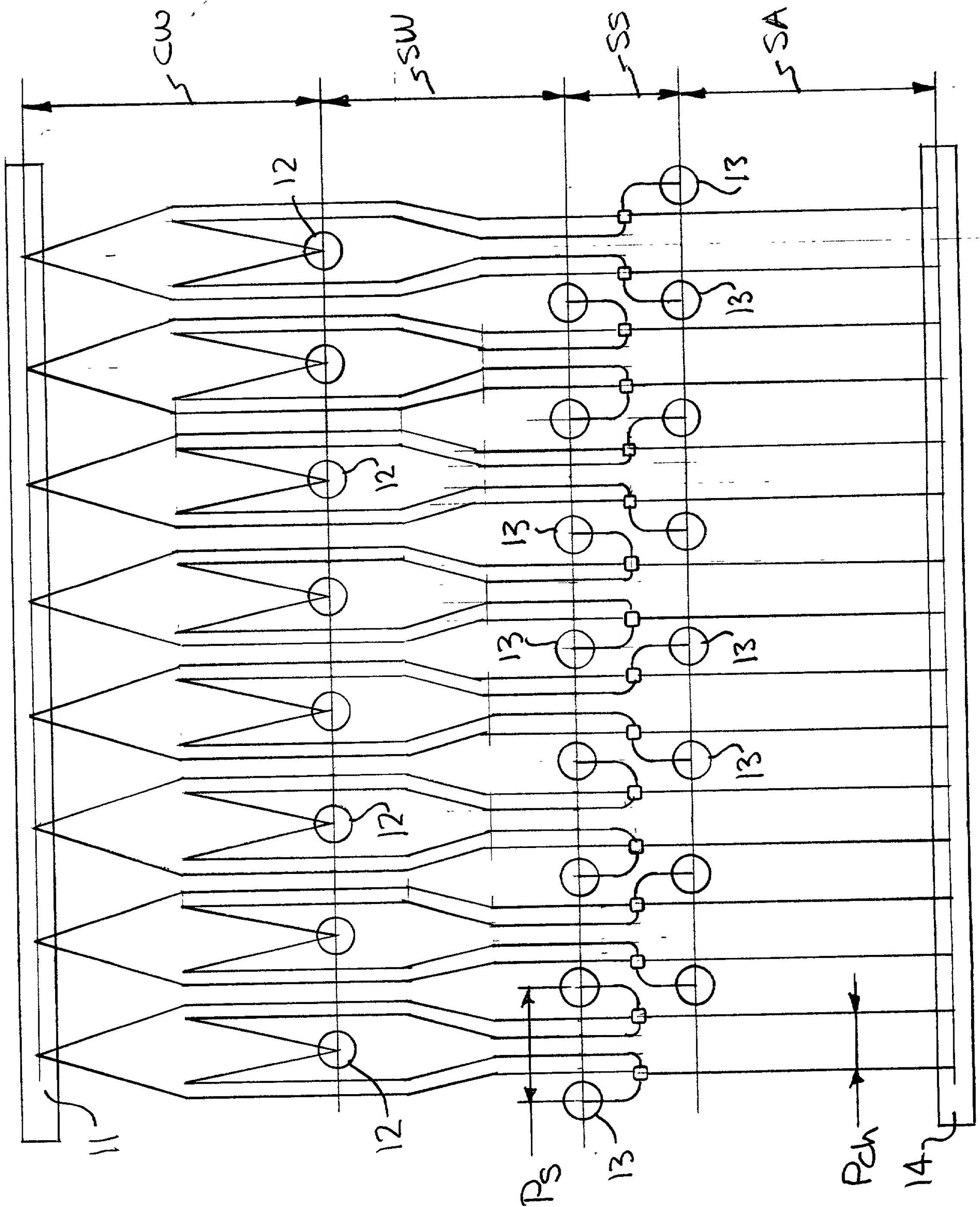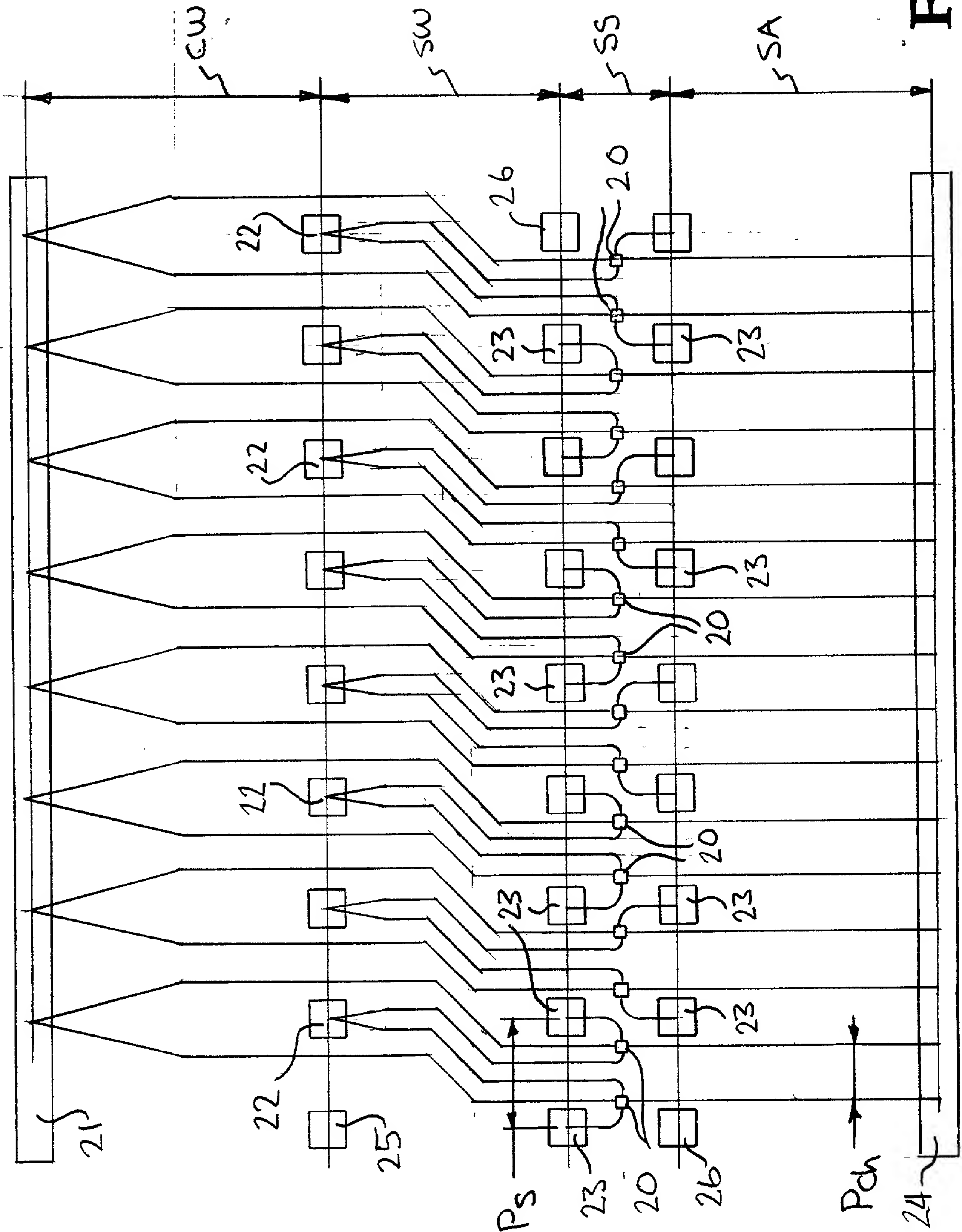
FIG. 4

COMBINED DECLARATION AND POWER OF ATTORNEY

X Declaration submitted
     with Initial Filing

❑ Declaration submitted
     after Initial Filing (surcharge
     (37 CFR 1.16(e)) required)

Attorney Docket: IL-10475
Applicant: Stefan P. Swierkowski
Serial No.:
Filing Date:

As a below named inventor(s), I (we) hereby declare that:

My (Our) residence, post office address and citizenship(s) are as stated below next to my (our) name(s).

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: <u>A MICROCHANNEL CROSS LOAD ARRAY WITH DENSE PARALLEL INPUT</u>

the specification of which (check one)
<u> X </u> is attached hereto   ____was filed on_____ as United States Application Number or PCT International Application Number_____
and was amended on _____(if applicable).

I (We) hereby state that I (we) have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I (We) acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I (We) hereby claim foreign priority benefits under 35, U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)   Priority Not Claimed
                                               ❑

_____
(Application Number)   (Country)   (Foreign Filing Date)
                                               ❑

_____
(Application Number)   (Country)   (Foreign Filing Date)

I (We) hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below:

_____

Application Serial No.   Filing Date

-1-

I (We) hereby claim the benefit under 35 U.S.C. 120 of any United States applications(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Application Serial No.	Filing Date	Status

POWER OF ATTORNEY: As the named inventor(s), I (we) hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Names	Registration No.	
Alan H. Thompson	29,981	
L. E. Carnahan	20,555	
Direct Correspondence To:	Direct Telephone Calls To:	
Alan H. Thompson	(Name and Telephone Numbers)	
Patent Attorney	Alan H. Thompson	
Lawrence Livermore National Laboratory	(925) 422-7820	
P.O. Box 808 - L-703		
Livermore, California 94551		

I (We) hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

STEFAN P. SWIERKOWSKI	*Stefan P. Swierkowski*
Full Name of Inventor	Signature
LIVERMORE, CALIFORNIA	*March 21, 2000*
Residence (City, State or Foreign Country)	Date
1655 WARSAW AVENUE, LIVERMORE, CALIFORNIA 94550	USA
Postal Address (Street, City, State, Zip Code	Citizenship
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	
Full Name of Inventor	Signature
Residence (City, State or Foreign Country)	Date
Postal Address (Street, City, State, Zip Code	Citizenship
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	